RF Design Example for MoCA 1.1 on ‘TiVo Mini’ STB

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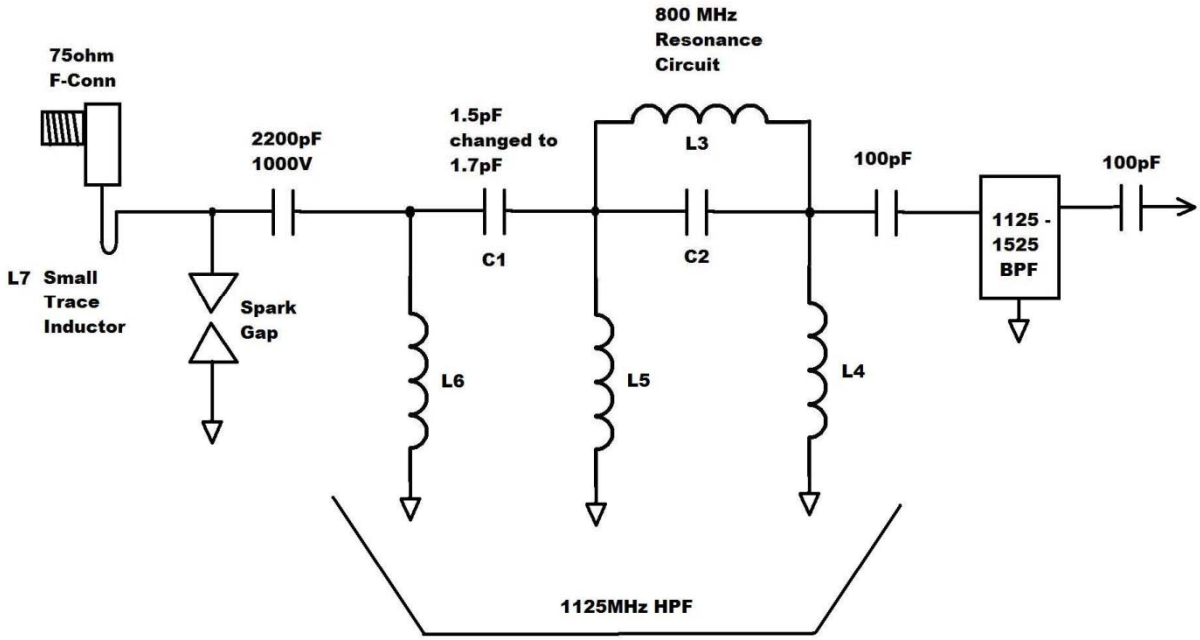

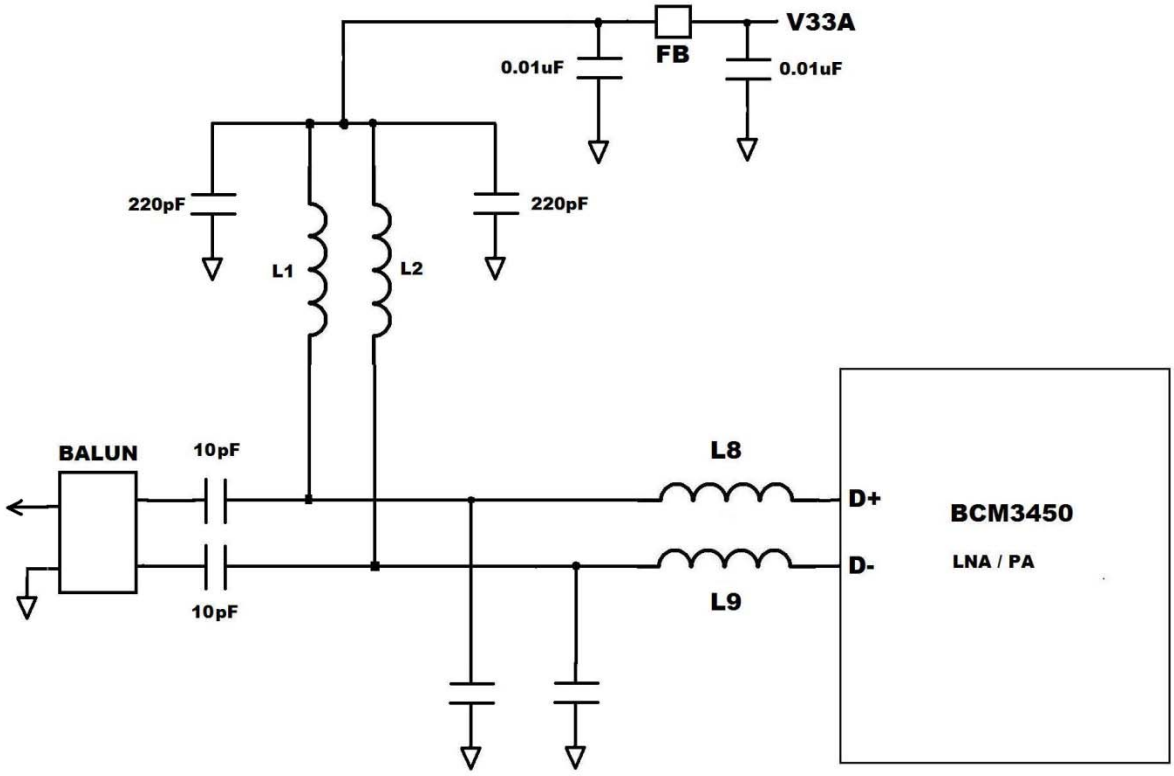

This MoCA 1.1 RF front end design was made to eliminate an 800MHz OOB spur caused by the PLL in the BCM7418 MoCA core, and a 125MHz OOB spur generated by the Gigabit IC elsewhere in the circuit. The Broadcom reference design board had only 1dB of margin at 800MHz. The circuit was designed and simulated with Sonnet SW running on a 16 core PC.

The tough part of the design was to reduce return-loss enough between 1125 – 1525MHz and have some margin. The MoCA 1.1 specification limit is -5dB across the band.

The board material is 1mm thick, 4-layer, FR-4 with a permittivity of 4.4 +/- 10%, and thickness variation of -10%/+15%. The S-parameters for the BCM3450 were not available so the D+/D- ports were assumed to be 50-ohm with 2pF pads. Trying to measure it directly did not give meaningful results.

The simulations had poor return-loss at 1125MHz until the L7 trace inductor was added.

After the new boards were manufactured the value of C1 had to be changed from 1.5pF to 1.7pF to maximize return-loss at 1125MHz and balance it against the return-loss at 1525MHz.

All test boards and pilot run sample boards had a return-loss of at least -7.5dB, and the 800MHz and 125MHz OOB spurs were eliminated.

The final MoCA 1.1 front end design passed all these PHY layer tests:

1. Transmit power
2. Frequency accuracy
3. Spectral Mask
4. Carrier Suppression
5. Carrier Phase Noise
6. OOB spurious from 54-864MHz
7. OOB spurious from 2-6GHz
8. Transmit return-loss
9. Receive return-loss
10. RX sensitivity PHYrate curve
11. 10E7 packet BER at 1dB above link loss
12. EVM max and shape